ABSTRACT

A shared memory switch architecture provides per-flow queuing that achieves high memory bandwidth and makes efficient use of memory. The memory of the memory switch is dynamically allocated to each port based on real-time traffic conditions. The priority of the packets is represented by queuing elements having a priority level determined by a weighted fair queue algorithm and its variants. The priority arbitration of queuing elements is made according to a two level hierarchy to increase the speed of priority queue management and therefore the switching throughput.